



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:

Paton et al.

Title:

OFFSET SPACER PROCESS FOR

FORMING N-TYPE

TRANSISTORS

Appl. No.:

10/619,877

Filing Date:

07/15/2003

Examiner:

Christy L. Novacek

Art Unit:

2822

CERTIFICATE OF EXPRESS MAILING I hereby certify that this correspondence is being deposited with the United States Postal Service's "Express Mail Post Office To Addressee" service under 37 C.F.R. § 1.10 on the date indicated below and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450. Ev 459171788 US 01/14/05 (Express Mail Label Number) (Date of Deposit) Roberta A. Cooper (Printed Name) Cooper (Signature)

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR §1.56

Mail Stop RCE Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

Submitted herewith on Form PTO/SB/08 is a listing of documents known to Applicants in order to comply with Applicants' duty of disclosure pursuant to 37 CFR §1.56.

A copy of each non-U.S. patent document and each non-patent document is being submitted to comply with the provisions of 37 CFR §1.97 and §1.98.

The submission of any document herewith, which is not a statutory bar, is not intended as an admission that such document constitutes prior art against the claims of the present application or that such document is considered material to patentability as defined in 37 CFR §1.56(b). Applicants do not waive any rights to take any action which would be appropriate to antedate or otherwise remove as a competent reference any document which is determined to be a *prima facie* art reference against the claims of the present application.



TIMING OF THE DISCLOSURE

The listed documents are being submitted in compliance with 37 CFR §1.97(b), within three (3) months of the filing date of the application.

RELEVANCE OF EACH DOCUMENT

The relevance of the foreign-language documents is described in an English-language abstract for the documents provided herewith. An English translation of the foreign-language documents is not readily available. However, the absence of such translation does not relieve the PTO from its duty to consider the submitted foreign language documents (37 CFR §1.98 and MPEP §609).

Applicants respectfully request that any listed document be considered by the Examiner and be made of record in the present application and that an initialed copy of Form PTO/SB/08 be returned in accordance with MPEP §609.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 CFR §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 06-1447. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 06-1447.

Respectfully submitted,

Date

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1/15/2005

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MODIFIED PTO/SB/08 (08-00)

Approved for use through 10/31/2002. OMB 0651-0031

U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Date Submitted: January 14, 2005

(use as many sheets as necessary)

Sheet 1 of 2

Complete if Known				
Application Number	10/619,877			
Filing Date	7/15/2003			
First Named Inventor	Eric N. Paton			
Group Art Unit	2822			
Examiner Name	Christy L. Novacek			
Attorney Docket Number	039153-0642 (H0970)			

U.S. PATENT DOCUMENTS							
Examiner Initials*	Cite No.1	U.S. Patent Docu	Kind Code ² (if	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
		US-2003/0153161		Chut et al.	08/14/2003		
		6,559,015		Yu	05/06/2003		
		US-2003/0068883		Ajmera et al.	04/10/2003		
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		5,825,066		Buynoski	10/20/1998		
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		4,784,718		Mitani et al.	11/15/1988		
		4,727,038		Watabe et al.	02/23/1988		
		4,745,082		Kwok	05/17/1988		

FOREIGN PATENT DOCUMENTS								
Examiner Initials*	Cite No. ¹	Foreign Patent Document Office ³ Number ⁴ Kind Code (if known)		Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶		
		10-270685	Japan	10/1998				
		5-160396	Japan	06/25/1993				
		4-123439	Japan	09/14/1990				
		3-248433	Japan	02/29/1990				

Examiner Signature		Date Considered	

^{*}EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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¹ Unique citation designation number. ²See attached Kinds of U.S. Patent Documents. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached.

MODIFIED PTO/SB/08 (08-00)

Approved for use through 10/31/2002. OMB 0651-0031

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	Substitute for	or form 1449B/	PTO		Complete if Known			
	INFORMAT	ON DISCLO	SURE	Application Number	10/619,877			
STATEMENT BY APPLICANT				Filing Date	7/15/2003			
Data Oakasiikada Januari 44,0005				First Named Inventor	Eric N. Paton			
Date Submitted: January 14, 2005			4, 2005	Group Art Unit	2822			
	(use as many	sheets as ne	cessary)	Examiner Name	Christy L. Novacek			
Sheet	2	of	2	Attorney Docket Number	039153-0642 (H0970)			

		NON PATENT LITERATURE DOCUMENTS	بنب
Examiner Initials*	Cite . No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	Ī
		International Electron Devices Meeting 1997, "Sub-100nm Gate Length Metal Gate NMOS Transistors Fabricated by a Replacement Gate Process" by Chatterjee et al, pages 821-824.	
		International Electron Devices Meeting 1999, "70nm MOSFET with Ultra-Shallow, Abrupt, and super-Doped S/D Extension Implemented by Laser Thermal Process (LTP)" by Yu et al, pages 509-512.	

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Examiner	•	[[Date	
Signature		(Considered	

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